10-23-00

A

Attorney Docket No. SAM-162
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BOX PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

NEW APPLICATION TRANSMITTAL

Transmitted herewith for filing is the patent application of

Inventor(s): Jang-Ho Cho

For (title): BRANCH PREDICTOR USING BRANCH PREDICTION ACCURACY HISTORY

CERTIFICATE OF MAILING
37 C.F.R. § 1.10
"Express Mail" Mailing Label Number EL675533035US
I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to BOX PATENT APPLICATION, Assistant Commissioner for Patents, Washington, DC 20231.
Date: 10/20 Elizabeth M Sumner
Elizabeth M. Sumner
Elizabeth M Sumner
Print Name

1. **Type of Application** This new application is for a(n)

☒ Original (nonprovisional)
☐ Design
☐ Plant
☐ Divisional.
☐ Continuation.
☐ Continuation-in-part (C-I-P).

2. **Benefit of Prior Application(s)**

☒ The new application being transmitted claims the benefit of prior Korean application(s) nos. 99-45786. See item 7 .

3. **Papers Enclosed**

8 Pages of specification
2 Pages of claims
1 Page of Abstract
2 Sheets of drawings
☒ formal
☐ informal
____ Page of Cover Sheet

☐ The **enclosed** drawing(s) are photograph(s), and there is also attached a "PETITION TO ACCEPT PHOTOGRAPH(S) AS DRAWING(S)." 37 C.F.R. 1.84(b).

4. **Additional papers enclosed**

☐ Preliminary Amendment

☐ Information Disclosure Statement (37 C.F.R. 1.98)

☐ Form PTO-1449 (PTO/SB/08A and 08B)

☐ Copies of cited references

☐ Declaration of Biological Deposit

☐ Submission of "Sequence Listing," computer readable copy and/or amendment pertaining thereto for biotechnology invention containing nucleoticle and/or amino acid sequence.

☐ Authorization of Attorney(s) to Accept and Follow Instructions from Representative

☐ Special Comments

☒ Other: Return Postcard.

5. Declaration or oath

☒ Enclosed

- ☐ Unexecuted
- ☒ Executed by
  - ☒ inventors
  - ☐ legal representative of inventor(s). 37 CFR 1.42 or 1.43.
  - ☐ joint inventor or person showing a proprietary interest on behalf of inventor who refused to sign or cannot be reached.
  - ☐ This is the petition required by 37 CFR 1.47 and the statement required by 37 CFR 1.47 is also attached. See item 12 below for fee.

☐ Not Enclosed

☐ Application is made by a person authorized under 37 C.F.R. 1.41 (c) on behalf of all the above named inventor(s).

- ☐ Showing that the filing is authorized.

6. Assignment

☒ An assignment of the invention to Samsung Electronics Co., Ltd.

☒ is attached. A separate ☐ "COVER SHEET FOR ASSIGNMENT (DOCUMENT) ACCOMPANYING NEW PATENT APPLICATION" or ☒ FORM PTO 1595 is also attached. will follow.

7. Certified Copy

Certified copy(ies) of application(s)

Country	Appln. no.	Filed
Korea	99-45786	21 October 1999

from which priority is claimed

☒ is (are) attached.

☐ will follow.

8. Fee Calculation (37 C.F.R. 1.16)

CLAIMS AS FILED				
	Number filed	Number Extra	Rate	Basic Fee 37 C.F.R. 1.16(a) **$710.00**
Total Claims (37 CFR 1.16(c))	8 - 20	0	$18.00	0
Independent Claims (37 CFR 1.16(b))	1 - 3	0	$80.00	0
Multiple dependent claim(s), if any (37 CFR 1.16(d))				

☐ A Preliminary Amendment canceling claims is enclosed. The filing fee is calculated based on the number of claims remaining after entry of the Preliminary Amendment.

☐ Amendment deleting multiple-dependencies is enclosed.

☐ Fee for extra claims is not being paid at this time.

Filing Fee Calculation $ 710.00

9. **Small Entity Statement(s)**

☐ Verified Statement(s) that this is a filing by a small entity under 37 CFR 1.9 and 1.27 is (are) attached.

☐ Status as a small entity was claimed in prior application _____, filed on_____ from which benefit is being claimed for this application under:

35 U.S.C. ☐ 119(e),
☐ 120,
☐ 121,
☐ 365(c),

and which status as a small entity is still proper and desired.

☐ A copy of the verified statement in the prior application is included.

Filing Fee Calculation (50% of A, B or C above)

$ 355.00

10. **Fee Payment Being Made at This Time**

☐ Not Enclosed

☐ No filing fee is to be paid at this time.
(This and the surcharge required by 3 7 C. F.R. 1.16(e) can be paid subsequently.)

☒ Enclosed

☒ Basic filing fee $ 710.00

☒ Recording assignment
($40.00; 37 C.F.R. 1.21(h))
(See attached "COVER SHEET FOR ASSIGNMENT ACCOMPANYING NEW APPLICATION".) $ 40.00

Total fees enclosed **$ 750.00**

11. **Method of Payment of Fees**

☒ Checks in the amounts of $ 710.00, 40.00

☐ Charge Account No. 19-0079 in the amount of $ _____
A duplicate of this transmittal is attached.

12. Authorization to Charge Additional Fees

☒ The Commissioner is hereby authorized to charge the following additional fees during the entire pendency of this application to Account No. 19-0079.

- ☒ 37 C.F.R. 1.16(a), (f) or (g) (filing fees)
- ☒ 37 C.F.R. 1.16(b), (c) and (d) (presentation of extra claims)
- ☐ 37 C.F.R. 1. 1 6(e) (surcharge for filing the basic filing fee and/or declaration on a date later than the filing date of the application)
- ☐ 37 C.F.R. 1.17 (application processing fees)
- ☐ 37 C.F.R. 1.18 (issue fee at or before mailing of Notice of Allowance, pursuant to 37 C.F.R. 1.311(b))

13. Instructions as to Overpayment

- ☒ Credit Account No. 19-0079
- ☐ Refund

Respectfully submitted,

Date: October 20, 2000

Samuels, Gauthier & Stevens, LLP
225 Franklin Street, Suite 3300
Boston, MA 02110
Telephone: (617) 426-9180, Ext. 149
Facsimile: (617) 426-2275

Steven M. Mills
Registration Number 36,610
Attorney for Applicant

K:\Samsung\162\pattransltr.wpd

PATENT
Attorney Docket No. SAM-162

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Jang-Ho Cho
Filing Date: Herewith
Title: Branch Predictor Using Branch Prediction Accuracy History

CERTIFICATE OF MAILING UNDER 37 C.F.R.§ 1.10

"Express Mail" Mailing Label Number EL675533035US I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated below and is addressed to BOX PATENT APPLICATION, Assistant Commissioner for Patents, Washington, DC 20231.

Oct. 20, 2000
Date

Lizabeth M. Sumner
Lizabeth M. Sumner

BOX PATENT APPLICATION
Assistant Commissioner for Patents
Washington, DC 20231

TRANSMITTAL LETTER

Sir:

Enclosed herewith for filing in the above-identified patent application please find the following listed items:

1. New Application Transmittal;
2. New Patent Application;
3. Executed Declaration, Petition and Power of Attorney;
4. Two (2) Sheets of Formal Drawings;
5. Certified Copy of Priority Document - Korean Application No 99-45786;
6. Check in the amount of $710.00 to cover requisite fee;
7. Assignment Recordation Form Cover Sheet - - PTO-1595;
8. Executed Assignment;
9. Check in the amount of $40.00 to cover assignment recordation fee; and
10. Return Postcard.

In connection with the foregoing matter, please charge any additional fees which may be due, or credit any overpayment, to Deposit Account Number 19-0079. A duplicate copy of this letter is provided for this purpose.

Respectfully submitted,

Date: October 20, 2000

Steven M. Mills
Registration Number 36,610
Attorney for Applicant

Samuels, Gauthier & Stevens, LLP
225 Franklin Street, Suite 3300
Boston, MA 02110
Telephone: (617) 426-9180, Ext. 149
Facsimile: (617) 426-2275
K:\Samsung\162\transapp.wpd

BRANCH PREDICTOR USING BRANCH PREDICTION ACCURACY HISTORY

This application relies for priority upon Korean Patent Application No. 1999-45786, filed on October 21, 1999, the contents of which are herein incorporated by reference in their entirety.

Field of the Invention

The present invention relates to the field of computer system, and more particularly to a branch predictor using branch prediction accuracy history and efficient processing techniques for instruction streams which include conditional program flow instructions, such as branch instructions.

Background of the Invention

Many microprocessors employ a technique known as hardware pipelining to increase instruction throughput by processing several instructions through different phases of execution concurrently. To maximize instruction execution efficiency, it is desirable to keep the instruction execution pipeline full (with an instruction being processed in each pipeline stage) as often as possible such that the pipeline produces useful output every clock cycle. However, whenever there has been a transfer of program flow control to another section of software code and instructions have been speculatively fetched and processed and it is determined that these instructions should not have been executed, the output from the pipeline is not useful.

Exceptions and program flow control instructions such as branch instructions provide examples of how the program flow control can be changed. Branch instructions, which may be conditional or unconditional and may transfer program flow control to a preceding or subsequent code section, are used for frequently encountered situations where a change in program flow control is desired.

A conditional branch instruction determines instruction flow based on the resolution of a specified condition. If A>B then branch to instruction X is an example of a conditional branch instruction. In this case, if A>B, program flow control branches to a code section beginning with instruction X, also referred to as the target code section. If A is not greater than B, the

instructions sequentially following the branch instruction in the program flow, referred to as the sequential code section, are executed. In executing such conditional branch instruction, it is required to check a condition of the branch instruction for determining the next instruction. Thus, performance of a microprocessor including a central processing unit (CPU) may be adversely affected in pipeline procedures of the microprocessor requiring fast instruction fetch.

To solve the aforementioned problem, many microprocessors adopt a branch predictor (or a branch prediction logic), which operates to predict the outcome of a branch instruction before identifying a condition check of the branch instruction, based on a predetermined branch prediction approach. Thus, instructions are then speculatively fetched from either the target code section or the sequential code section based on the prediction indicated by the branch predictor. Therefore, a pipeline stall can be prevented. However, when a branch prediction is missed, many instructions from the incorrect code section may be in various stages of processing in the instruction execution pipeline. On encountering such a misprediction, instructions following the mispredicted conditional branch instruction in the pipeline (or multiple pipelines) are flushed, and instructions from the other correct code section are fetched. Flushing the pipeline creates bubbles or gaps in the pipeline. Several clock cycles may be required before the next useful instruction completes execution, and before the instruction execution pipeline produces useful output. Such an incorrect guess causes the pipeline to stall until it is refilled with valid instructions. This delay is called the mispredicted branch penalty.

To reduce above described misprediction ratio, various kinds of branch predictors are used. Among the branch predictors, a two-level branch predictor is likely to become more common. A P6 processor of Intel Corporation is the first to use a two-level branch algorithm to improve accuracy. This algorithm, first published by Tse-Yu Yeh and Yale Patt, has the potential to push accuracy well beyond the 90% level achieved by the best processors today.

Fig. 1 is a schematic diagram for illustrating a structure of a conventional two-level branch predictor. For example, the branch predictor is illustrated in Fig. 2 of *New Algorithm Improves Branch Prediction* by Linley Gwennap, March 27, 1995, MOCROPROCESSOR, pp. 17-21.

Referring to **Fig. 1**, the two-level branch predictor is composed of a branch history

register (BHR) **10** and a pattern history table (PHT) **20**. The branch history register **10** is used for recording the actions of the most recent k conditional branches. For example, a 1 stored in the branch history register **10** may denote a branch taken , and a 0 stored in the branch history register **10** may denote a branch not taken , respectively. The performed k conditional branches are called a pattern.

The pattern history table **20** is used for recording a pattern history bit **Sc**, which is used for predicting a conditional branch of a branch instruction to be performed in response to each pattern. For example, the two-level branch predictor predicts a conditional branch **I(Sc)** in response to an entry of 10 stored in the pattern history table **20**. The entry corresponds with a pattern 111010 stored in the branch history register **10**. According to the predicted conditional branch **I(Sc)**, the next instruction to the branch instruction is fetched. Referring to the Gwennap paper referenced above, a predicted conditional branch **I(Sc)** is determined by a most significant bit (MSB) of a pattern history bit **Sc** stored in the pattern history table **20**.

For example, on the assumption that a real conditional branch of the branch instruction is **Rc**, if a predicted conditional branch **I(Sc)** is different from the real conditional branch **Rc**, this case is called a prediction miss. In this case, execution of instructions following the mispredicted conditional branch **I(Sc)** are withdrawn.

According to the real conditional branch **Rc**, both data of the branch history register **10** and the pattern history bit **Sc** stored in the pattern history table **20** are changed. This process is described as follows. When a least significant bit (LSB) corresponding to the real conditional branch **Rc** of the branch instruction is stored to the branch history register **10**, the remaining bits are shifted to the left. At this time, the pattern history bit **Sc** stored in the pattern history table **20** is updated in response to the real conditional branch **Rc**. For example, if the real conditional branch **Rc** is 1 denoting predict taken , the pattern history bit **Sc** is increased by 1 , and if the real conditional branch **Rc** is 0 denoting predict not taken , the pattern history bit **Sc** is decreased by 1 . The pattern history bit **Sc** can be composed of an up/down saturating counter as shown in *A Study of Branch Prediction Strategies* , by J. Smith, May 1981, pp. 135-148. The saturating counter maintains a minimal value of a pattern history bit **Sc** when the pattern history bit **Sc** is the minimal value, although the real conditional branch **Rc** is 0 denoting not taken . In

addition, the saturating counter maintains a maximum value of a pattern history bit **Sc** when the pattern history bit **Sc** is the maximum value, although the real conditional branch **Rc** is 1 denoting taken .

Although branch prediction accuracy may be improved or turned by using different branch prediction algorithms, mispredictions still occur. By the time a misprediction is identified, many instructions from the incorrect code section may be in various stages of processing in the instruction execution pipeline.

An example of a solution to the forgoing performance penalty relevant to mispredicting is disclosed in U.S. Pat. No. 5,860,017 to Sharangpani et al., issued on Jan. 12, 1999, entitled, "Processor and Method for Speculatively Executing Instructions from Multiple Instruction Streams Indicated by a Branch Instruction," which identifies branch instructions, which in relationship to other conditional branch instructions, have a relatively high likelihood of being mispredicted. In this case, once a condition in a branch instruction is identified as being unlikely to be predicted accurately, the processor fetches and decodes instructions from both target and sequential instruction streams indicated by the conditional branch instruction. However, the method proposed by Sharangpani et al. may cause performance deterioration by a resource conflict and may lead to high hardware cost, since the processor fetches both target and sequential instruction streams. Therefore, there is a need for a branch predictor capable of efficient processing of branch instructions by reducing prediction miss with a comparatively simple circuit configuration and low hardware cost.

Summary of the Invention

It is therefore an object of the present invention to provide a branch predictor capable of efficiently processing branch instructions by reducing prediction misses with a comparatively simple circuit configuration and low hardware cost.

According to an aspect of the present invention, there is provided a branch predictor which includes branch prediction means for predicting a conditional branch of a branch instruction. A comparator generates a comparison signal by comparing the predicted conditional branch from the branch prediction means with a real conditional branch of the branch instruction.

An accuracy history table stores an accuracy history of the predicted conditional branch. A first state transition logic generates an accuracy history bit to be stored to the accuracy history table in response to the comparison signal. A multiplexer outputs either the conditional branch or an inverted conditional branch as a final branch prediction outcome, in response to a predicted accuracy history signal based on the accuracy history bit.

Brief Description of the Drawings

The foregoing and other objects, features and advantages of the invention will be apparent from the following more particular description of preferred embodiments of the invention, as illustrated in the accompanying drawings in which like reference characters refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the invention.

Fig. 1 is a schematic diagram illustrating a structure of a conventional two-level branch predictor.

Fig. 2 is a schematic diagram illustrating a structure of one embodiment of a two-level branch predictor according to the present invention.

Description of the Preferred Embodiment

In accordance with the invention, a branch predictor outputs either a predicted conditional branch or an inverted predicted conditional branch as a final branch prediction outcome, in response to a predicted accuracy history signal based on an accuracy history bit. According to the accuracy history bit, it is determined whether the branch prediction outcome of the branch predictor is correct. If the predicted conditional branch is correct, the branch predictor outputs the predicted conditional branch, and if the predicted conditional branch is not correct, the branch predictor outputs the inverted predicted conditional branch, in response to the predicted accuracy history signal.

Fig. 2 is a schematic diagram illustrating a structure of one embodiment of a two-level branch predictor according to the present invention. Referring to **Fig. 2**, the two-level branch predictor comprises a branch history register **15** for recording actions of the most recent k

conditional branches, a pattern history table **25** for recording a pattern history bit **Sc** used for generating a predicted conditional branch **I(Sc)**, and an accuracy history table **60** for recording accuracy history of the predicted conditional branch **I(Sc)**. The accuracy history table **60** is composed of a memory array.

A first state transition logic circuit **30** generating a pattern history bit **Sc** to be stored to the pattern history table **25** in response to a real conditional branch **Rc** is coupled to the pattern history table **25**. In addition, a second state transition logic circuit **50** generating an accuracy history bit **Ac** to be stored to the accuracy history table **60** is coupled to the accuracy history table **60**.

Further, the branch predictor according to the present invention comprises a comparator **40** generating a comparison signal by comparing the predicted conditional branch **I(Sc)** generated by the pattern history bit **Sc** with the real conditional branch **Rc** of the branch instruction. The comparison signal is inputted to the second state transition logic circuit **50** to generate the accuracy history bit **Ac**. In addition, the branch predictor comprises a multiplexer **70** selecting either a predicted conditional branch **I(Sc)** or an inverted predicted conditional branch as a final branch prediction outcome or result. A predicted accuracy history signal **I(Ac)** based on the accuracy history bit **Ac** is used as a selection signal for the multiplexer **70**. Operation of the branch predictor is described as follows.

A predicted conditional branch **I(Sc)** is generated in response to a pattern history bit **Sc** corresponding to a pattern stored in the branch history register **15**. The predicted conditional branch **I(Sc)** is inputted to the comparator **40** to be compared with a real conditional branch **Rc**.

The real conditional branch **Rc** has a 1 or 0 value according to "predict taken" or "predict not taken," respectively , and the value stored in the branch history register **15** is updated in response to the value of the real conditional branch **Rc**. According to the updated value of the branch history register **15**, the pattern history bit **Sc** is updated. The first state transition logic circuit **30** updates the pattern history bit **Sc**. The first state transition logic circuit **30** is composed of an up/down saturating counter. In the first state transition logic circuit **30**, the value of the pattern history bit **Sc** is increased by 1 when the real conditional branch **Rc** is 1 (i.e., taken), and the value of the pattern history bit **Sc** is decreased by 1 when the real conditional branch **Rc** is 0

(i.e., not taken).

The predicted conditional branch **I(Sc)** has a value of 1 or 0 in response to a most significant bit (MSB) of the pattern history bit **Sc**. The comparator **40** outputs 1 or 0 as a comparison signal to the second state transition logic circuit **50** by comparing the real conditional branch **Rc** and the predicted conditional branch **I(Sc)**. For example, if the predicted conditional branch **I(Sc)** is the same as the real conditional branch **Rc**, the comparator **40** outputs 1 , and if the predicted conditional branch **I(Sc)** is different from the real conditional branch **Rc**, the comparator **40** outputs 0 .

The second state transition logic circuit **50** receiving the comparison signal determines an accuracy history bit **Ac** to be stored to the accuracy history table **60** in response to the comparison signal. The second state transition logic circuit **50** is composed of an up/down saturating counter increasing the value of the accuracy history bit **Ac** by 1 when the predicted conditional branch **I(Sc)** is the same as the real conditional branch **Rc**, and decreasing the value of the accuracy history bit **Ac** by 1 when the predicted conditional branch **I(Sc)** is different from the real conditional branch **Rc**. The accuracy history bit **Ac** can be used after learning a branch accuracy of the corresponding pattern by monitoring the pattern.

According to the above described method, the accuracy history bit **Ac** is determined and stored to the accuracy history table **60**. According to the accuracy history bit **Ac**, it can be determined whether a prediction result of the branch predictor is correct. For example, if a pattern history bit **Sc** is 011 corresponding to a pattern 11 10 stored in the branch history register **15**, a predicted accuracy history signal **I(Ac)** is generated by an MSB of the accuracy history bit **Ac**. The predicted accuracy history signal **I(Ac)** is used for determining whether the predicted conditional branch **I(Sc)** is correct. For example, if it is considered as the predicted conditional branch **I(Sc)** is correct, the predicted accuracy history signal **I(Ac)** having a value of 1 is outputted to the multiplexer **70**. Thus, the predicted conditional branch **I(Sc)** is outputted from the multiplexer **70** as a final prediction result. In addition, if it is considered as the predicted conditional branch **I(Sc)** is not correct, the predicted accuracy history signal **I(Ac)** having a value of 0 is outputted to the multiplexer **70**. Thus, the inverted predicted conditional branch is outputted from the multiplexer **70** as a final prediction result. As described above, the predicted

accuracy history signal **I(Ac)** is used as a selection signal of the multiplexer **70** selecting either the predicted conditional branch **I(Sc)** or an inverted predicted conditional branch as a final prediction outcome of the branch predictor.

As described above, the branch predictor according to the present invention outputs either a predicted conditional branch or an inverted predicted conditional branch as a final branch prediction outcome, in response to a predicted accuracy history signal based on an accuracy history bit, so that the two-level branch predictor can reduce the misprediction and a microprocessor can process branch instructions more efficiently. In this case, the branch prediction according to the present invention merely appends the accuracy history table **60** and multiplexer **70** to the conventional branch predictor. Thus, the branch prediction according to the present invention can reduce the misprediction with relatively simple circuitry and low hardware cost.

While this invention has been particularly shown and described with references to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the following claims.

What is claimed is:

CLAIMS

1. A branch predictor comprising:

branch prediction means for predicting a conditional branch of a branch instruction;

a comparator for generating a comparison signal by comparing the predicted conditional branch from the branch prediction means with a real conditional branch of the branch instruction;

an accuracy history table for storing an accuracy history of the predicted conditional branch;

a first state transition logic circuit for generating an accuracy history bit to be stored to the accuracy history table in response to the comparison signal; and

a multiplexer for outputting an alternative one of the conditional branch and an inverted conditional branch as a final branch prediction outcome, in response to a predicted accuracy history signal based on the accuracy history bit.

2. The branch predictor according to claim 1, wherein the branch prediction means comprises:

a branch history register for storing conditional branches of previous branch instructions;

a pattern history table for storing pattern history bits used for generating the predicted conditional branch corresponding to the conditional branches of the previous branch instructions stored in the branch history register; and

a second state transition logic circuit for generating the pattern history bits in response to the real conditional branch of the branch instruction.

3. The branch predictor according to claim 2, wherein the second state transition logic circuit includes an up/down saturating counter.

4. The branch predictor according to claim 1, wherein the accuracy history table includes a memory array.

5. The branch predictor according to claim 1, wherein the comparator generates the comparison signal having a first logic value when the predicted conditional branch is the same as the real conditional branch, and generates the comparison signal having a second logic value when the predicted conditional branch is different from the real conditional branch.

6. The branch predictor according to claim 1, wherein the first state transition logic circuit includes an up/down saturating counter.

7. The branch predictor according to claim 6, wherein the first state transition logic circuit is used after learning the predicted branch accuracy of patterns of previous branch instructions.

8. The branch predictor according to claim 1, wherein the predicted accuracy signal is determined by a most significant bit of the accuracy history bit.

BRANCH PREDICTOR USING BRANCH PREDICTION ACCURACY HISTORY

Abstract of the Disclosure

A branch predictor outputs either a predicted conditional branch or an inverted predicted conditional branch as a final branch prediction outcome, in response to a predicted accuracy history signal based on an accuracy history bit. According to the accuracy history bit, it is determined whether the branch prediction outcome of the branch predictor is correct. If the predicted conditional branch is correct, the branch predictor outputs the predicted conditional branch, and if the predicted conditional branch is not correct, the branch predictor outputs the inverted predicted conditional branch, in response to the predicted accuracy history signal. For performing this process, the branch prediction appends an accuracy history table and a multiplexer to a conventional branch predictor, so that the branch prediction according to the present invention can reduce the misprediction with relatively simple circuitry and low hardware cost.

Fig. 1

(Prior Art)

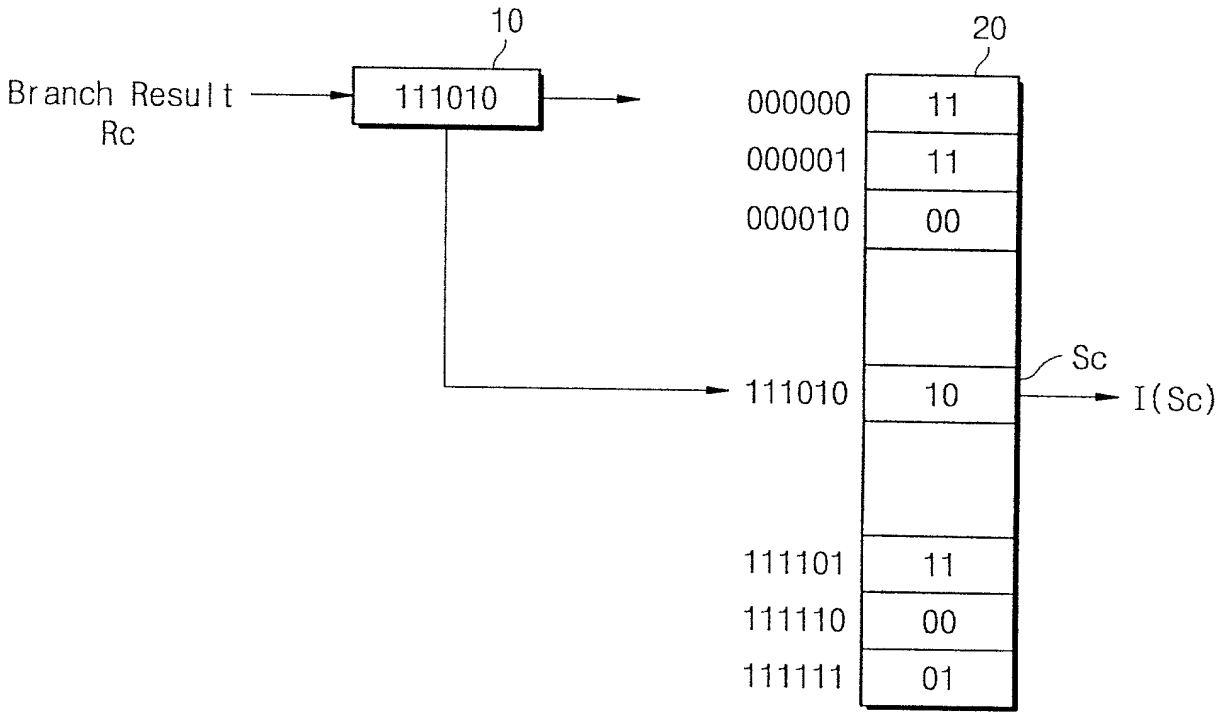
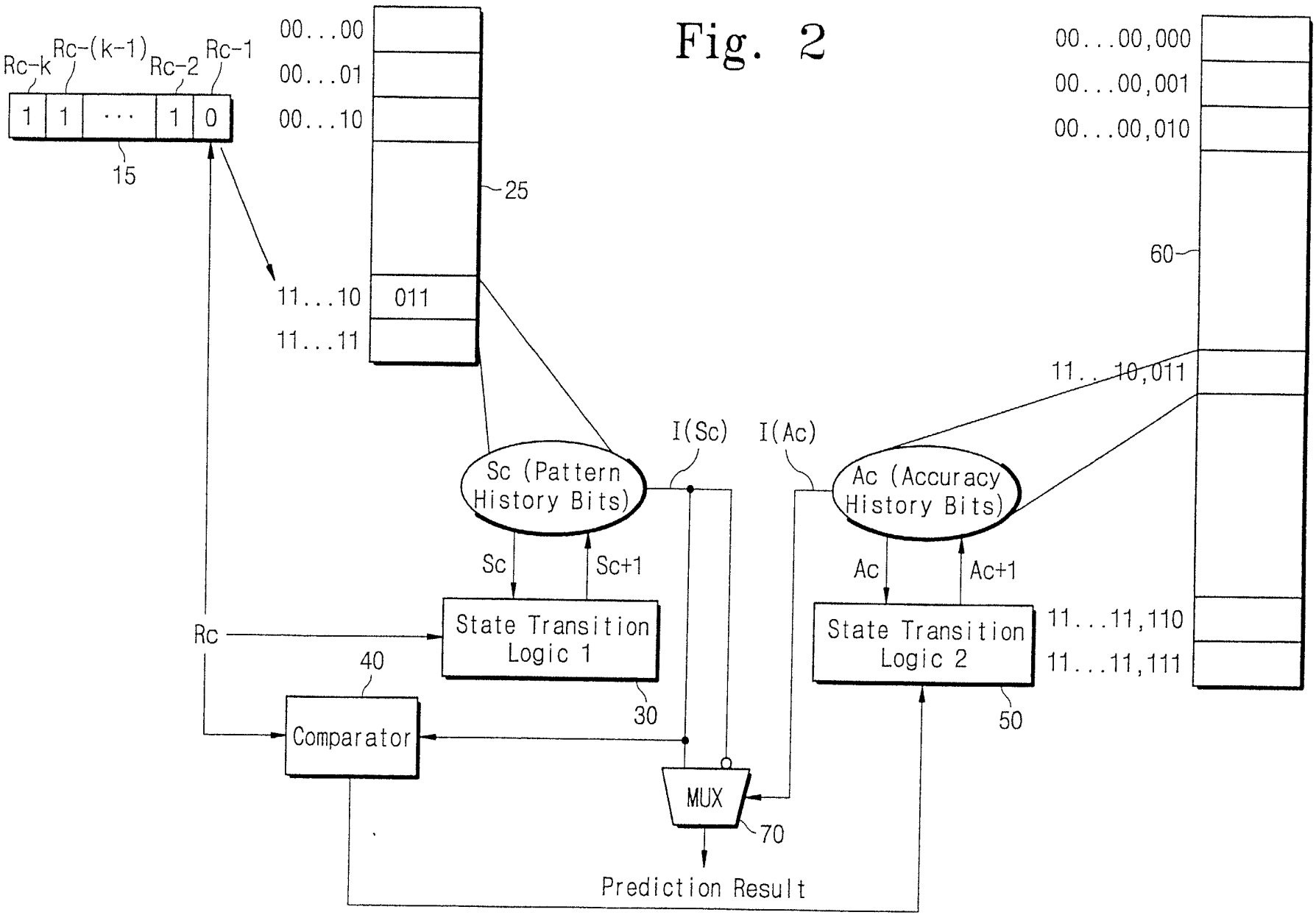


Fig. 2


Rc-k
Rc-(k-1)
Rc-2
Rc-1
1
1
...
1
0
15
00...00
00...01
00...10
11...10
011
11...11
25
00...00,000
00...00,001
00...00,010
60
11...10,011
11...11,110
11...11,111
I(Sc)
I(Ac)
Sc (Pattern History Bits)
Ac (Accuracy History Bits)
Sc
Sc+1
Ac
Ac+1
Rc
State Transition Logic 1
State Transition Logic 2
30
50
40
Comparator
MUX
70
Prediction Result

DECLARATION, PETITION AND POWER OF ATTORNEY FOR PATENT APPLICATION	Attorney Docket No: SAM-162

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Branch Predictor Using Branch Prediction Accuracy History

the specification of which (check only one):

__X__ is attached hereto.

_____ was filed as United States Patent Application

Serial No. _____

on _____

and was amended

on _____

(if applicable)

_____ was filed as PCT Patent Application

Serial No. _____

on _____

and was amended under PCT Article 19

on _____

(if applicable)

I hereby state that I have reviewed and understand the contents of the specification, including the claims as amended by any amendment referred to herein.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

PRIOR FOREIGN/PCT APPLICATION(S) AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. § 119:

COUNTRY (if PCT indicate PCT)	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 35 U.S.C. § 119 (YES/NO)
Republic of Korea	99-45786	21 October 1999	YES

DECLARATION, PETITION AND POWER OF ATTORNEY FOR PATENT APPLICATION	Attorney Docket No: SAM-162

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

PRIOR U.S. APPLICATIONS FOR BENEFIT UNDER 35 U.S.C. § 119(e):

APPLICATION NUMBER	FILING DATE

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or PCT international application(s) designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56 which occurred between the filing date of the prior applications and the national or PCT international filing date of this application:

PRIOR U.S. APPLICATIONS OR PCT INTERNATIONAL APPLICATION(S) DESIGNATING THE U.S. FOR BENEFIT UNDER 35 U.S.C. § 120:

APPLICATION NUMBER (if PCT indicate PCT)	DATE OF FILING (day, month, year)	STATUS: (PATENTED, PENDING OR ABANDONED)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorneys and/or agents to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

Maurice E. Gauthier	Reg. No. 20,798	Patrick J. O'Shea	Reg. No. 35,305
Richard L. Stevens	Reg. No. 24,445	Arlene J. Powers	Reg. No. 35,985
Matthew P. Connors	Reg. No. 39,298	Steven M. Mills	Reg. No. 36,610
William E. Hilton	Reg. No. 35,192	Anthony P. Onello, Jr.	Reg. No. 38,372

Send Correspondence to:	Direct Telephone Calls to:
Steven M. Mills, Esq. Samuels, Gauthier & Stevens LLP 225 Franklin Street Boston, Massachusetts 02110	Steven M. Mills, Esq. (617) 426-9180 Ext. 149 (617) 426-2275 (facsimile)

Wherefore I petition that letters patent be granted to me for the invention or discovery described and claimed in the attached specification and claims, and hereby subscribe my name to said specification and claims and to the foregoing declaration, power of attorney, and this petition.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Signature	Jung-Ho Cho	Date	Oct. 20, 2000

Full Name of 1st Inventor	Family Name Cho	First Given Name Jung-Ho	Second Given Name
Residence & Citizenship	City Suwon, Kyunggi-do	State or Foreign Country Republic of Korea	Country of Citizenship Republic of Korea
Post Office Address	Post Office Address 3-111, Hanshwan Apt., 462, Kwon-dong, Kwonsun-ku	City Suwon, Kyunggi-do	State & Zip Code/Country Republic of Korea